ABSTRACT

POWER EFFICIENT SYMBOL PROCESSING

5   The present invention is related to a symbol rate processing system for high-speed spread spectrum communications arranged for operation at a specific data rate, comprising programmable hardware blocks running at specific clock frequencies, characterised in that said
10   system comprises programmable registers comprising means for interleaving, means for error correction and means for rate matching, wherein said clock frequencies are significantly less than the frequencies needed in a DSP-centric approach.

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(Figure 1)